Game Boy CPU Architecture in 5 minutes

Which Game Boy?

CPU Overview

- **Sharp LR35902** - heavily based on Zilog Z80 but with a limited instruction set and some Game Boy specific additions
  - **8-bit processor** running at **4.19 MHz**.
  - 16-bit memory address space
  - **Dual-bus architecture**, allowing simultaneous instruction fetch and data access.
  - **Interrupt handling**, events can trigger execution changes.
  - **Power efficiency**, contributes to the 30 hour battery life of the device.
  - **No dedicated multiplication or division instructions**.

Registers

15 . . . 8	7 . . . 0
A (Accumulator)	F (Flags)
B	C
D	E
H	L

15 . . . 0
SP (Stack pointer)
PC (Program counter)

7	6	5	4	3	2	1	0
Z	N	H	C	0	0	0	0

Z - Zero Flag
N - Subtract Flag
H - Half Carry Flag
C - Carry Flag
0 - Not used, always zero

Instruction Set

- Supports **arithmetic, logic, bitwise operations, conditional jumps, and memory operations**.
- **Cycle timings vary**: Instructions generally execute in **4 to 16 clock cycles**
- **Interrupt-driven execution** with five interrupt sources:
  - **VBlank** – Triggered when the screen finishes drawing
  - **LCDC** – Triggered by the LCD controller for screen updates.
  - **Timer** – Triggered by the internal timer for timing operations.
  - **Serial** – Triggered by serial data communication.
  - **Joypad** – Triggered when the user presses a button on the Game Boy.

Hello World?

```
LD A, $41          ; Load ASCII 'A' into register A
LD (0xC000), A  ; Store it in memory
HALT                ; Stop execution
```